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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,591	10/17/2003	Dong-Hyun Kim	8028-28 (SPX200208-0017US	2255

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	**PAPER NUMBER**
1756	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,591	KIM ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

In response to the Remarks of 9/6/05 the examiner withdraws the prior office action rejections and includes new rejections here.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims as written are unclear.

The preamble recites -a phase edge phase shift mask enforcing a width of a field gate image- and further comprising: a phase shift mask comprises a plurality of shifters.

The use of the language of a mask "enforcing a width" is unclear. Also the phrase "a phase shift mask comprising a phase shift mask" is unclear or redundant.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Cho et al. (6,593,038) or Lukanc et al. (6,749,971) or Park et al. (US 20040043305).

Cho et al. teach (see claims) a set of masks for generating trim to be used in conjunction with phase shifters during an optical lithography process for manufacturing an

integrated circuit, comprising: a first mask; a phase shifter within the first mask that produces a region of destructive light interference on a photoresist layer; wherein the phase shifter in the first mask is used to expose a first polysilicon line in a gate region of a first transistor in the integrated circuit; wherein dimensions of the phase shifter satisfy design rules; a second mask; trim within the second mask to be used in conjunction with the first mask; wherein the trim in the second mask is used to protect the first polysilicon line from exposure during use of the second mask; wherein the trim is derived from the previously-defined dimensions of the phase shifter while ensuring that the design rules are satisfied; and a second polysilicon feature defined within the second mask and in close proximity to a portion of the trim located on one side of the first polysilicon line, such that if the portion of the trim were of a default size a design rule violation would occur between the portion of the trim and the second polysilicon feature; wherein the portion of the trim is derived to be less that the default size so that the design rule violation.

Cho et al. also teach as can be seen in FIG. 1A, when two phase shifters are located in close proximity to each other, conflicts can arise. In FIG. 1A, a first phase shifter comprising a zero-degree phase region 102 and a 180-degree phase region 104 is used to produce a small line width in a gate region 103 of polysilicon line 101. Similarly, a second phase shifter comprising a zero-degree phase region 114 and a 180-degree phase region 112 is used to produce a small line width in a gate region 113 of polysilicon line 111.

Lukanc et al. teach (see claims) a method of designing a phase shifting mask, the method comprising: (a) identifying edges of a first phase region of a phase shifting mask, the first phase region being located proximate a critical region and the identified edges not being edges of the first phase region adjacent to the critical region; (b) expanding the

identified edges outwardly and inwardly to define a narrow line along the edges of the first phase region; and (c) forming chrome in the narrow line to form a chrome boundary along the edges of the first phase region.

And wherein the narrow line has a width of a minimum gate width dimension.

And further comprising: (a) assigning phase polarities to the first phase region; (b) defining edges of the first phase region; (c) establishing a boundary around the defined edges; and (d) assigning area outside of the established boundary to have phase zero.

And further comprising generating a trim mask to remove undesired patterns between the first phase region and the second phase region.

And further comprising generating a trim mask to remove undesired patterns between regions of first and second phases.

Park et al. teach a set of masks for manufacturing a highly-integrated circuit device comprising: an alternating phase shifting mask (APSM) comprising: first and second phase shifting areas defining an access interconnection line, the first and second phase shifting areas having different phases and being disposed adjacent to each other to generate destructive light interference; and a first opaque pattern formed on a first transparent substrate to define the first and second phase shifting areas; and a halftone phase shifting trim mask (HPSTM) comprising: a second opaque pattern formed on a second transparent substrate to prevent the access interconnection line from being erased; and a halftone pattern that defines a pass interconnection line connected to the access interconnection line.

And wherein the second opaque pattern corresponding to the first and second phase shifting areas includes: a main block pattern disposed between the first and second phase

shifting areas, the main block pattern having a plurality of edges, the edges being separated from corresponding edges of the first and second phase shifting areas by a misalignment margin required when double exposing the APSM and the HPSTM; and a sub-block pattern that extends from the main block pattern corresponding to the access interconnection line and prevents the access interconnection line from being erased.

And wherein the access interconnection line forms an access gate of an active device, and a line width of the main block pattern is greater than a line width of an active area of the active device.

And wherein the sub-block pattern extends from ends of the main block pattern, and further extends outwardly from the edges of the first and second phase shifting areas by no more than the wavelength of an exposure source used for the set of masks.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho et al. (6,593,038) or Lukanc et al. (6,749,971) or Park et al. (US 20040043305) in view of Cote et al. (6,787,271).

The claimed invention is directed to a phase edge phase shift mask and a method of fabricating a phase edge phase shift mask, the mask controlling a width of a field gate

image, comprising: a phase shift mask which comprises a plurality of shifters and an opaque region for defining the shifters; and a trim mask which comprises first, second, and third trim patterns overlapped with the phase shift mask, wherein the first trim pattern corresponds to an opaque region between the shifters, the second trim pattern is connected to the first trim pattern and is separated from at least one shifter having a predetermined width, and the third trim pattern is in contact with selected sides of the first and the second trim patterns.

And wherein the third trim pattern contacts the first and the second trim patterns to prevent the formation of a notch structure.

And wherein a region separated by a predetermined width between the shifters and the first and the second trim patterns is protected by the third trim pattern. wherein a dummy pattern is attached to the second trim pattern along a side opposite to the selected sides of the second trim pattern in contact with the first and third trim patterns.

The applicant states that if a width of the notch structure is out of specification as compared to the tolerances as defined by a design rule at the check point (1P), an inspection process detects the notch structure as a defect. If light is transmitted through the portion of the notch structure that overlaps the photoresist of the trim mask (35) during a photo exposure process, an unwanted field gate image (not shown) is formed by sensitizing the photoresist (29) on the semiconductor substrate (25) of FIG. 1b.

[0020] The rough image (41-1) is formed when light passes through the notch structure on the trim mask (35) of FIG. 1c during an exposure process. Thus, the rough image (41-1) can be transferred to a gate having a very narrow width causing an increase in

the resistance and drops in the current driving capability in a gate. In other words, the performance of the gate on the semiconductor device deteriorates.

The teachings of Cho et al. or Lukanc et al. or Park et al. differ from those of the applicant in that the applicant teaches the use of a the third trim pattern in contact with selected sides of first and second trim patterns in order to prevent the formation of a notch structure.

Cote et al. teach a method for defining a full phase layout for defining a layer of material in an integrated circuit. The method can be used to define, arrange, and refine phase shifters to substantially define the layer using phase shifting. Through the process, computer readable definitions of an alternating aperture, dark field phase shift mask and of a complimentary mask are generated.

Masks can be made from the definitions and then used to fabricate a layer of material in an integrated circuit. The separations between phase shifters, or cuts, are designed for easy mask manufacturability while also maximizing the amount of each feature defined by the phase shifting mask. Cost functions are used to describe the relative quality of phase assignments and to select higher quality phase assignments and reduce phase conflicts.

Cote et al. also teach (see col. 8, lines 35-45) -

FIG. 9 illustrates a similar configuration to that found in FIG. 7 however here, the two original shifters, the shifter 920 and the shifter 910 adjacent to the feature 720 and the feature 900, respectively, are abutting one another leaving notches, the notch 930 and the notch 932. Some embodiments of the invention merge the shifters and fill such notches, as

shown by the dashed lines. The width of the filled notch corresponds to the length over which the two shifters are less than, or equal to, d.sub.4 apart in some embodiments.

It would have been obvious to one having ordinary skill in the art to take the teachings of Cho et al. or Lukanc et al. or Park et al. and combine them with the teachings of Cote et al. in order to make the claimed invention because it is known in the art to use trim masks to decrease the width of gates and to control the transfer of a pattern during exposure by blocking regions such as the notch area that would be considered undesirable.

Applicant's arguments with respect to claim1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
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Art Unit 1756

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10/21/05